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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,397	09/26/2005	Young-Min Choi	AB-1408 US	2205

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EXAMINER	
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ART UNIT	PAPER NUMBER
2871	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,397	CHOI ET AL.	
	Examiner	Art Unit	
	Nathanael R. Briggs	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishikawa et al. (US 7,119,870).

4. Regarding claims 1 and 10, Nishikawa discloses an LCD (see figures 4, 6, 8 and 16, for instance) having a first insulating substrate (10); a gate wire (51) formed on the first insulating substrate (10) and including a gate line (55), a gate electrode (11) connected to the gate line (55), and a gate pad connected to the gate line (55); a storage electrode wire (52) formed on the first insulating substrate (10) and including a storage electrode line (52) and a storage electrode (53) branched from the storage electrode lines (52); a gate insulating layer (12) formed on the gate wire (11) and the storage electrode wire (52); an amorphous silicon layer (13) formed on the gate insulating layer (12); a contact layer (14) formed on the amorphous silicon layer (13); a

data wire (54) formed on the contact layer (14) and including a data line (54) intersecting the gate line (55), a data pad connected to the data line (54), a source electrode (13s) connected to the data line (54) and located adjacent to the gate electrode (11), and a drain electrode (13) located opposite the source electrode (13s) with respect to the gate electrode (11); a passivation layer (17) formed on the data wire (54); a pixel electrode (19) formed on the passivation layer (17), connected to the drain electrode (16); a second insulating substrate (30) facing the first insulating substrate (10): a black matrix (32) formed on the second insulating layer (30) and defining a pixel area; a color filter (31) formed on the pixel area; and a common electrode (34) formed on the color filter (31); a first cutout pattern (93) formed on the first insulating substrate (10) and a second cutout pattern (36) formed on the second insulating substrate (30) and partitioning a pixel region (19) into a plurality of domains along with the first cutout pattern (93), wherein each of the domains has a width equal to or less than 30 μm (*claim 1,* column 8, lines 48-51), of the second cutout pattern (36) is equal to or less than 24 microns (*claim 9,* column 8, lines 48-51), the pixel electrode (19) has a chamfered edge (see figure 8), and wherein at least one of the first and second cutout patterns (36, 93) has at least one oblique portion and at least one branch extending from the oblique portion (see figure 4, 36, 36a, 36c). Claims 1 and 10 is therefore unpatentable.

5. Regarding claim 11, Nishikawa discloses the LCD of claim 10 (see figures 4, 6, 8 and 16, for instance), further comprising a liquid crystal layer (21) interposed between the first insulating substrate (10) and the second insulating substrate (30), wherein liquid

to the first insulating substrate (10) in absence of electric field (column 8, lines 7-10). Claim 11 is therefore unpatentable.

6. Regarding claim 12, Nishikawa discloses the LCD of claim 11 (see figures 4, 6, 8 and 16, for instance), wherein the width of the second cutout pattern (36) is equal to or less than 5 microns (column 8, lines 48-51). Claim 12 is therefore unpatentable.

7. Regarding claim 13, Nishikawa discloses the LCD of claim 11 (see figures 4, 6, 8 and 16, for instance), wherein the width of the first (93) and the second (36) cutout patterns is equal to or less than cell gap of the liquid crystal layer (21). Claim 13 is therefore unpatentable.

8. Regarding claims 2 and 14, Nishikawa discloses the LCD of claims 1 and 11 (see figures 4, 6, 8 and 16, for instance), wherein the first (93) and the second (36) cutout patterns partition a pixel region into a plurality of domains (column 11, lines 4-7), and the width of the domains is equal to or less than 28 microns (column 8, lines 48-51). Claims 2 and 14 is therefore unpatentable.

9. Regarding claims 3 and 15, Nishikawa discloses the LCD of claims 2 and 14 (see figures 4, 6, 8 and 16, for instance), wherein the width of the domains is equal to or less than 22 microns (column 8, lines 48-51). Claims 3 and 15 are therefore unpatentable.

10. Regarding claims 4 and 16, Nishikawa discloses the LCD of claim 15 (see figures 4, 6, 8 and 16, for instance), wherein the width of the domains is equal to or less than 17 microns (column 8, lines 48-51). Claims 4 and 16 are therefore unpatentable.

11. Regarding claim 5, Nishikawa discloses the LCD of claim 1 (see figures 4, 6, 8 and 16, for instance), wherein the first cutout pattern (93) includes a cutout provided at

the pixel electrode (19) and the second cutout pattern (36) includes a cutout provided at the common electrode (34). Claim 5 is therefore unpatentable.

12. Regarding claim 6, Nishikawa discloses the LCD of claim 1 (see figures 4, 6, 8 and 16, for instance), wherein the width of the second cutout pattern (36) is equal to or less than 24 microns (column 8, lines 48-51). Claim 6 is therefore unpatentable.

13. Regarding claim 7, Nishikawa discloses the LCD of claim 6 (see figures 4, 6, 8 and 16, for instance), wherein the width of the second domain partitioning member (36) is equal to or less than 5 microns (column 8, lines 48-51). Claim 7 is therefore unpatentable.

14. Regarding claim 8, Nishikawa discloses the LCD of claim 1 (see figures 4, 6, 8 and 16, for instance), wherein an extension of the domains makes an angle of 45 degrees or 135 degrees with the gate line (11). Claim 8 is therefore unpatentable.

15. Regarding claim 9, Nishikawa discloses the LCD of claim 1 (see figures 4, 6, 8 and 16, for instance), wherein the data line (54) has a triple-layered structure including an amorphous silicon layer, a doped amorphous silicon layer, and a metal layer. Claim 9 is therefore unpatentable.

16. Regarding claim 17, Nishikawa discloses the LCD of claim 11 (see figures 4, 6, 8 and 16, for instance), further comprising an overcoat (33) interposed between the color filter (31) and a common electrode (34). Claim 17 is therefore unpatentable.

17. Regarding claim 18, Nishikawa discloses the LCD of claim 1 (see figures 4, 6, 8 and 16, for instance), wherein the width of each of the domains is in the range of 9 to 30 microns (column 8, lines 48-51). Claim 18 is therefore unpatentable.

18. Regarding claim 19, Nishikawa discloses the LCD of claim 1 (see figures 4, 6, 8 and 16, for instance), wherein the width of the second domain partitioning member is in the range of 9 to 15 microns (column 8, lines 48-51). Claim 18 is therefore unpatentable.

19. Regarding claim 20, Nishikawa discloses the LCD of claim 11 (see figures 4, 6, 8 and 16, for instance), wherein the first and the second cutout patterns (36, 93) partition a pixel region (19) into a plurality of domains, each having a width in the range of 9 to 30 microns (column 8, lines 48-51). Claim 20 is therefore unpatentable.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathanael R. Briggs whose telephone number is (571) 272-8992. The examiner can normally be reached on 9 AM - 5:30 PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nathanael Briggs
5/11/07

ANDREW SCHECHTER
PRIMARY EXAMINER